Hard Implementation of the Euclidian Distance Using Translinear CMOS Circuits

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Abstract

In this paper I present an analog CMOS current-mode circuit for calculating the Euclidian Distance. This citcuit represents one of the main computation blocks in the hard implementation of the SVM (Support Vector Machine) image classifing algorithm. The circuit will be used in a Pspice simulation environment for VLSI circuits. Simulations have been performed proving the validity of design and circuit functionality.